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Fig. 1

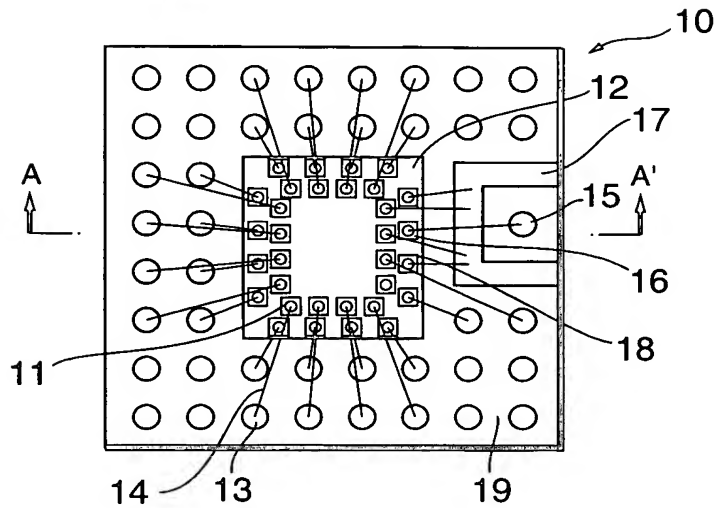


Fig. 2

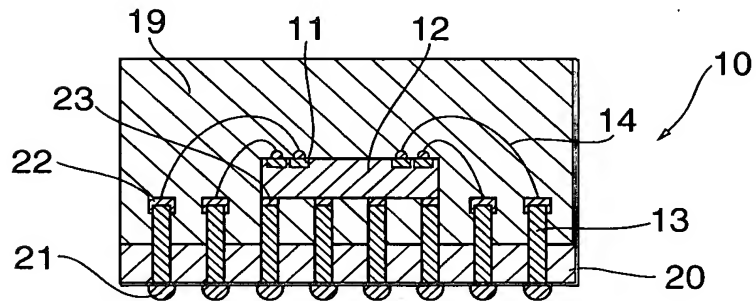
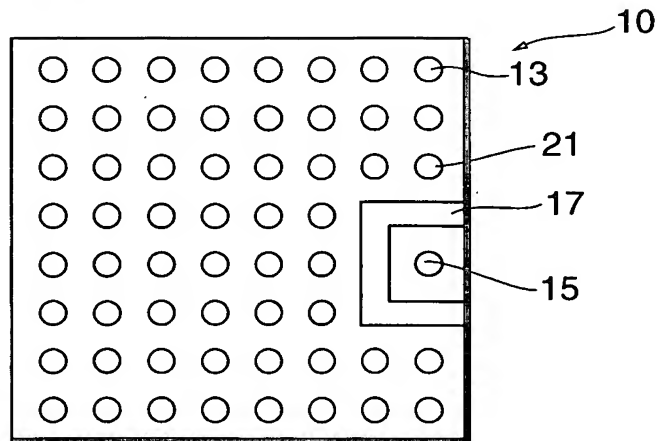


Fig. 3



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Fig. 4

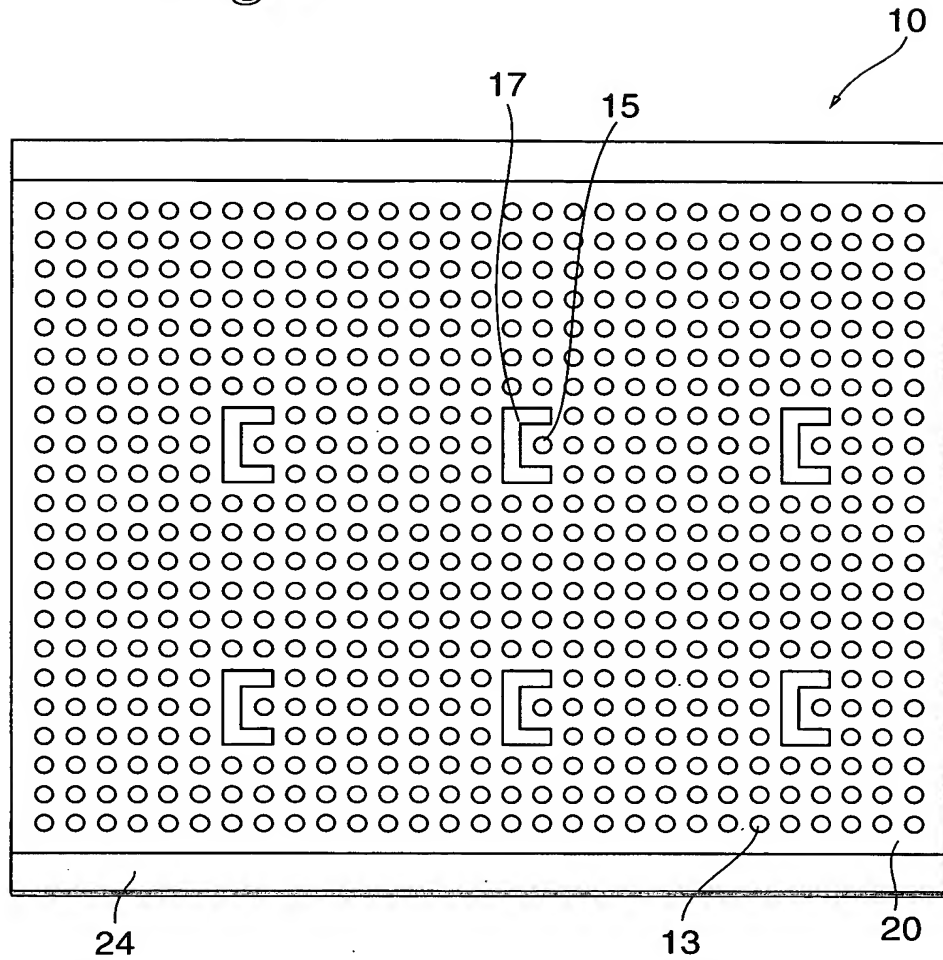


Fig. 5

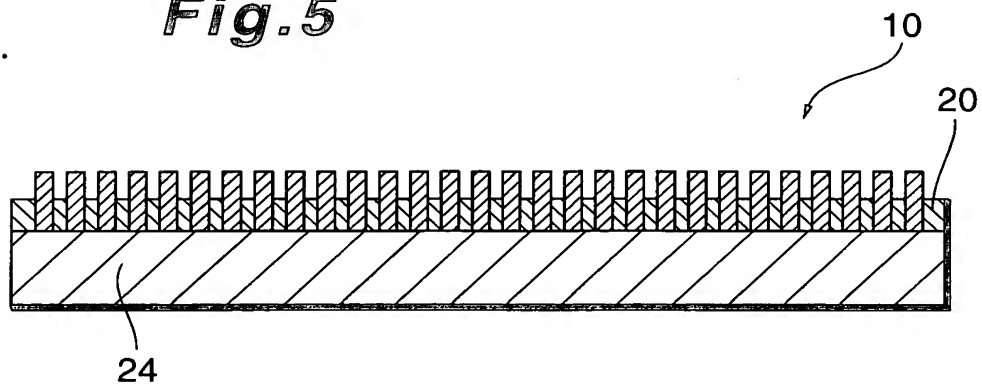
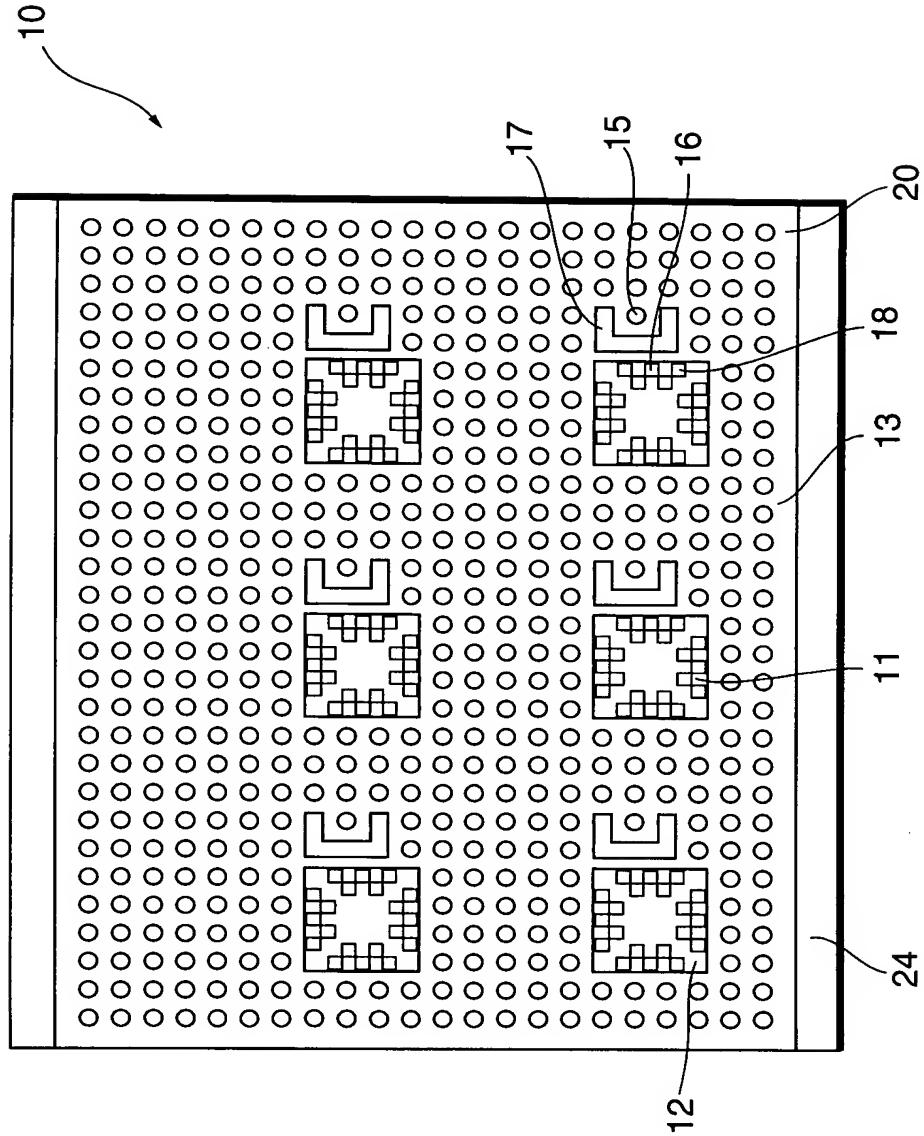


Fig.6



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Fig.7

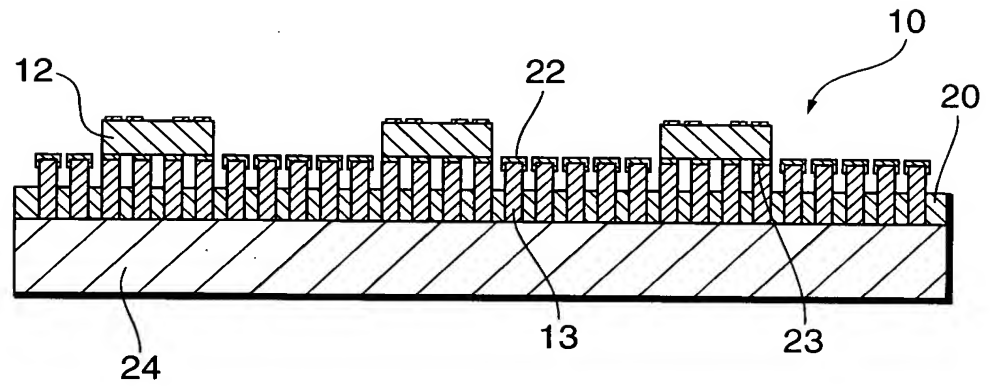
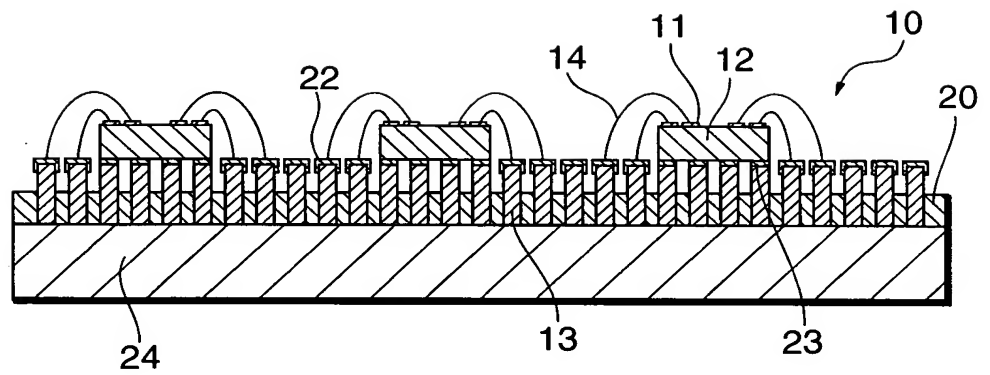
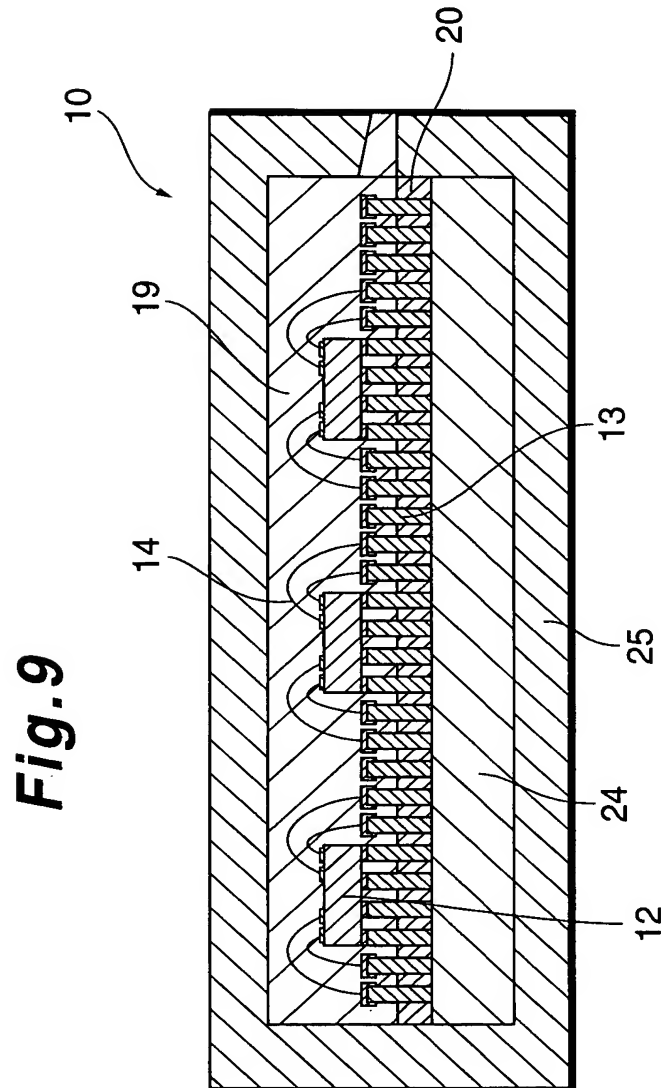


Fig.8



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Fig. 10

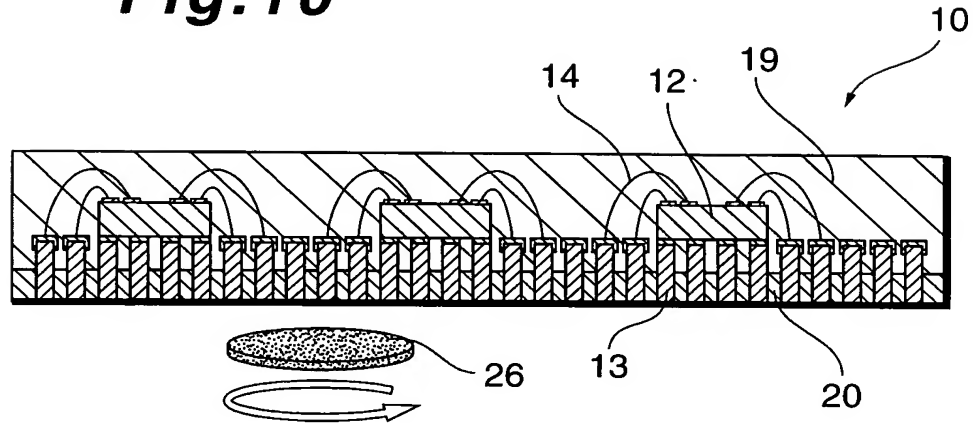
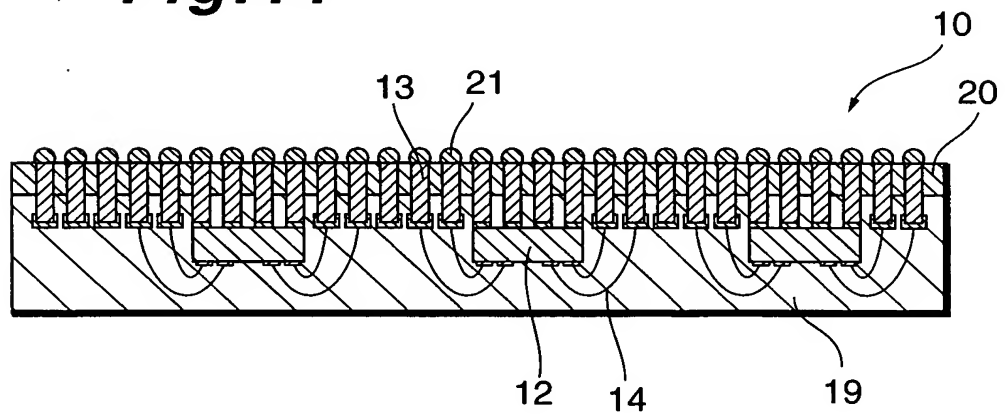


Fig. 11



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Fig.12

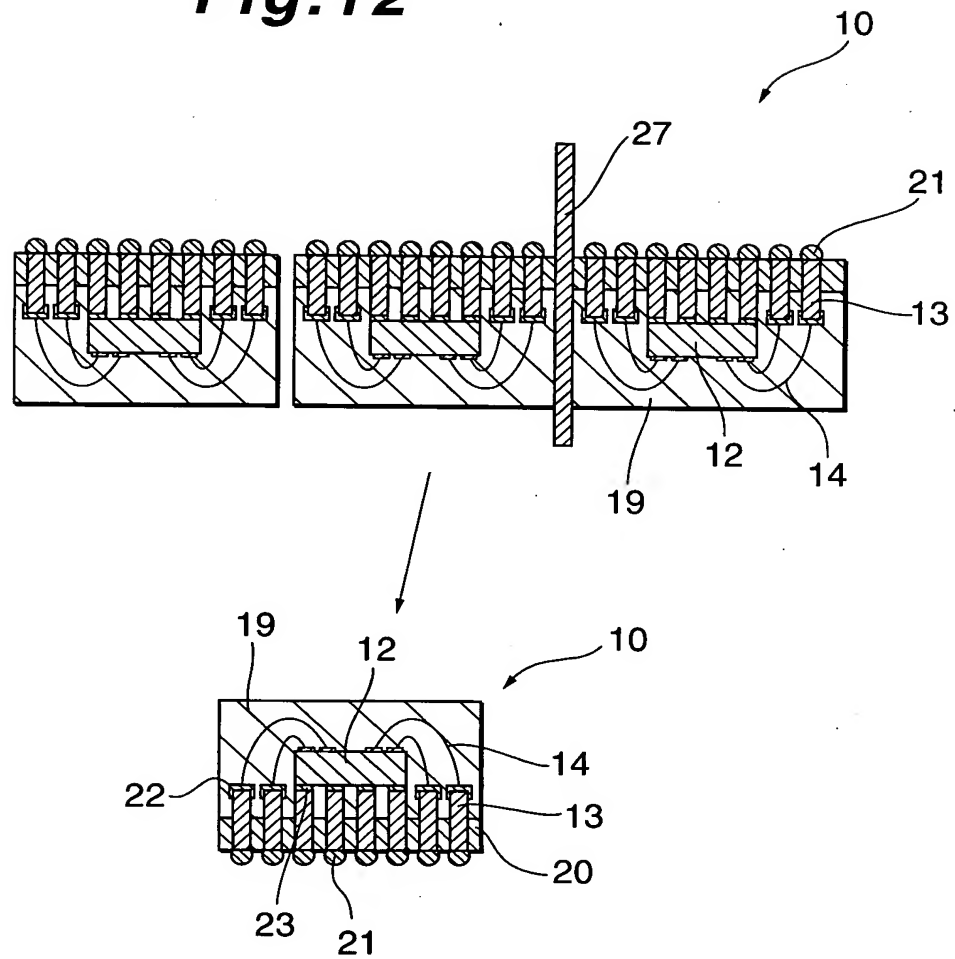
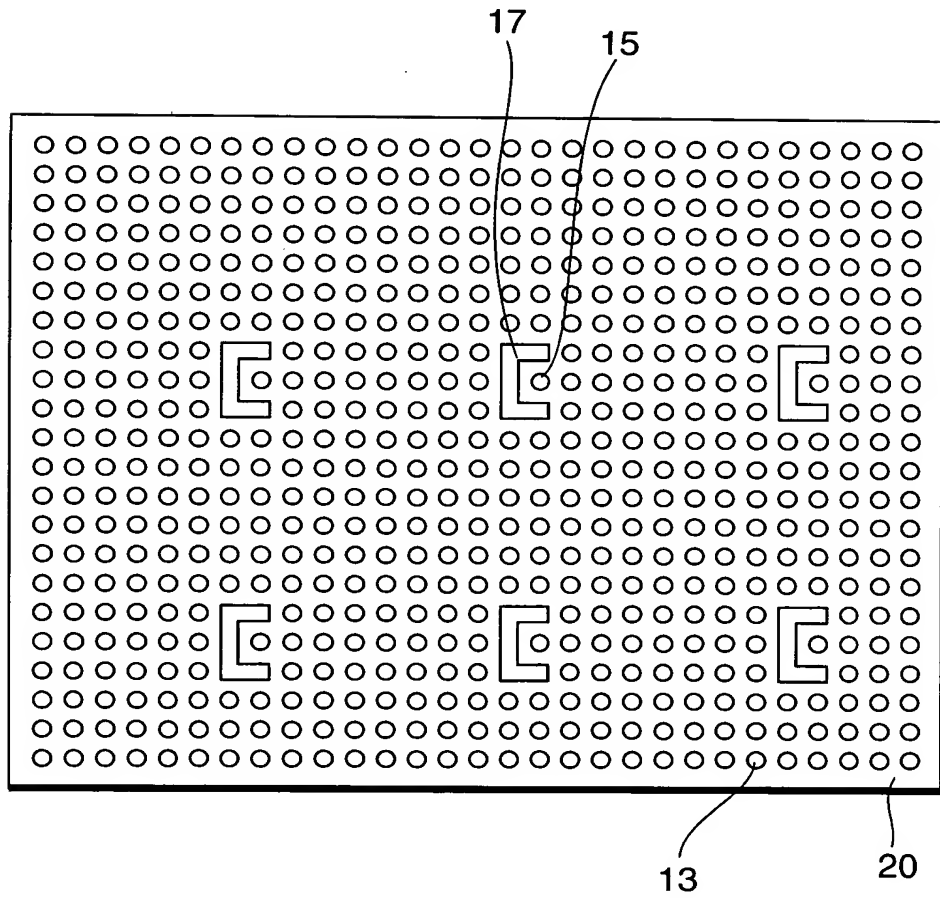


Fig. 13



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Fig. 14

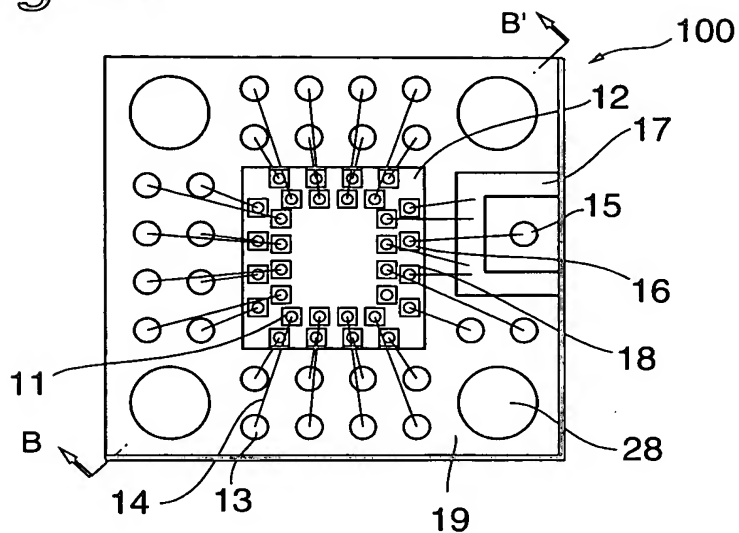


Fig. 15

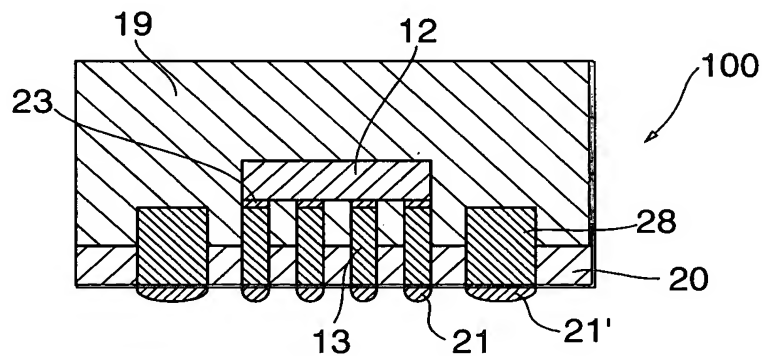
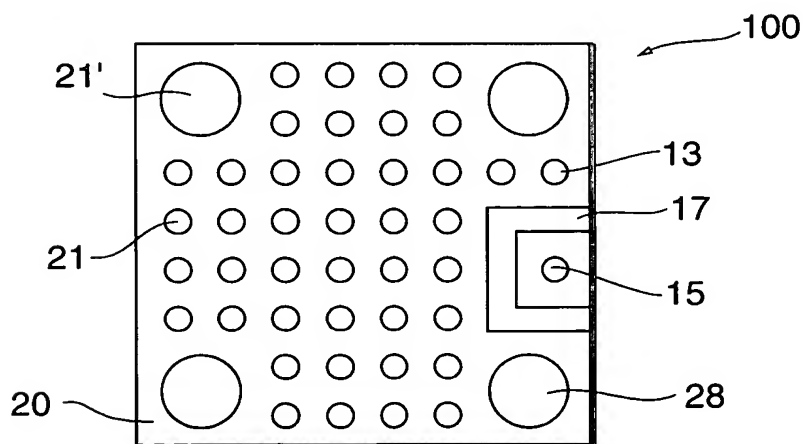


Fig. 16



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Fig. 17

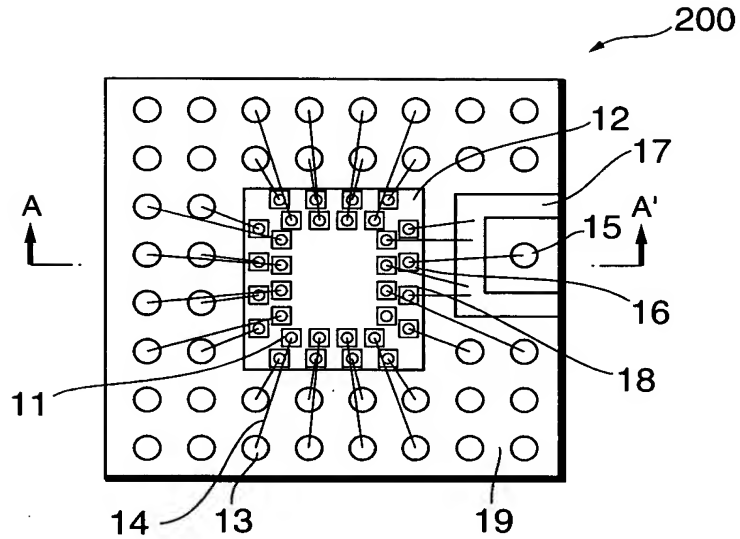


Fig. 18

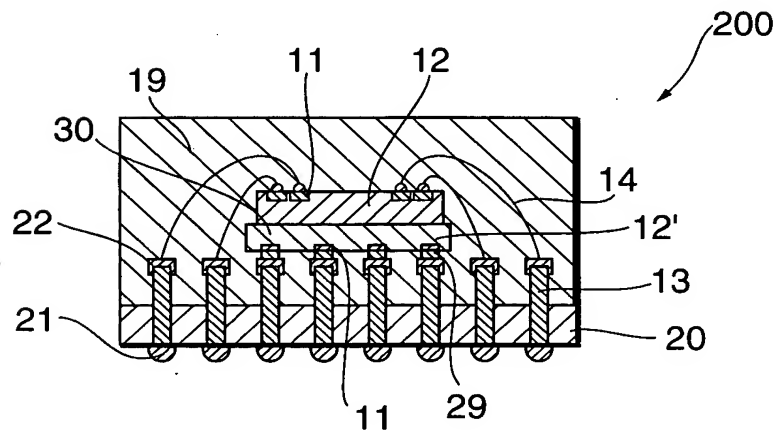


FIG. 1 is a schematic diagram of a square device 300. The device features a central square region 11, which contains a grid of small squares 12. This central region is surrounded by a ring of larger circles 13. The entire device is enclosed in a square frame 14. A coordinate system is shown with A and B axes. A smaller coordinate system A' and B' is also shown, centered on the central region. Other labels include 15, 16, 17, 18, 19, 28, and 300.

A cross-sectional view of a semiconductor device 300. The device features a substrate 19 with a top surface 11 and a bottom surface 12. A layer 14 is formed on the top surface 11. A series of vertical structures 22 are formed on the bottom surface 12. A layer 23 is formed on the top surface 11, covering the structures 22. A layer 32 is formed on the bottom surface 12, also covering the structures 22. A layer 13 is formed on the bottom surface 12, underlying the structures 22. A layer 14 is formed on the top surface 11, covering the structures 22. A layer 23 is formed on the top surface 11, covering the structures 22. A layer 32 is formed on the bottom surface 12, also covering the structures 22. A layer 13 is formed on the bottom surface 12, underlying the structures 22.

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Fig.21

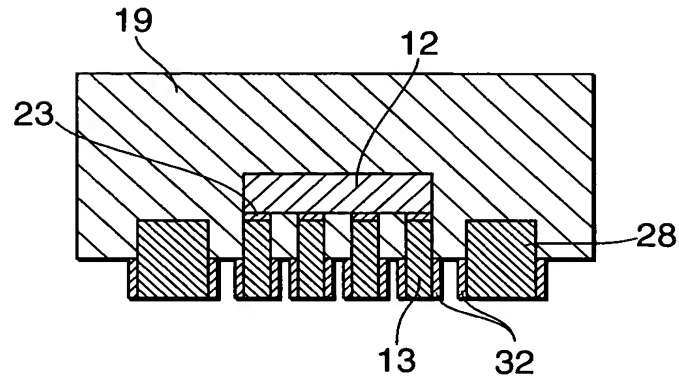
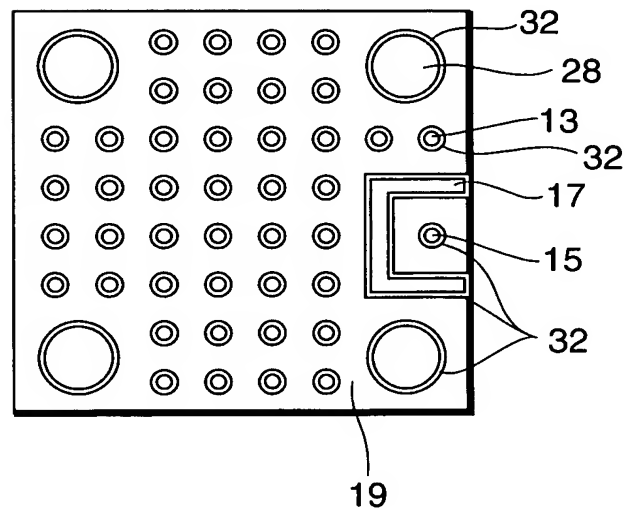


Fig.22



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Fig.23

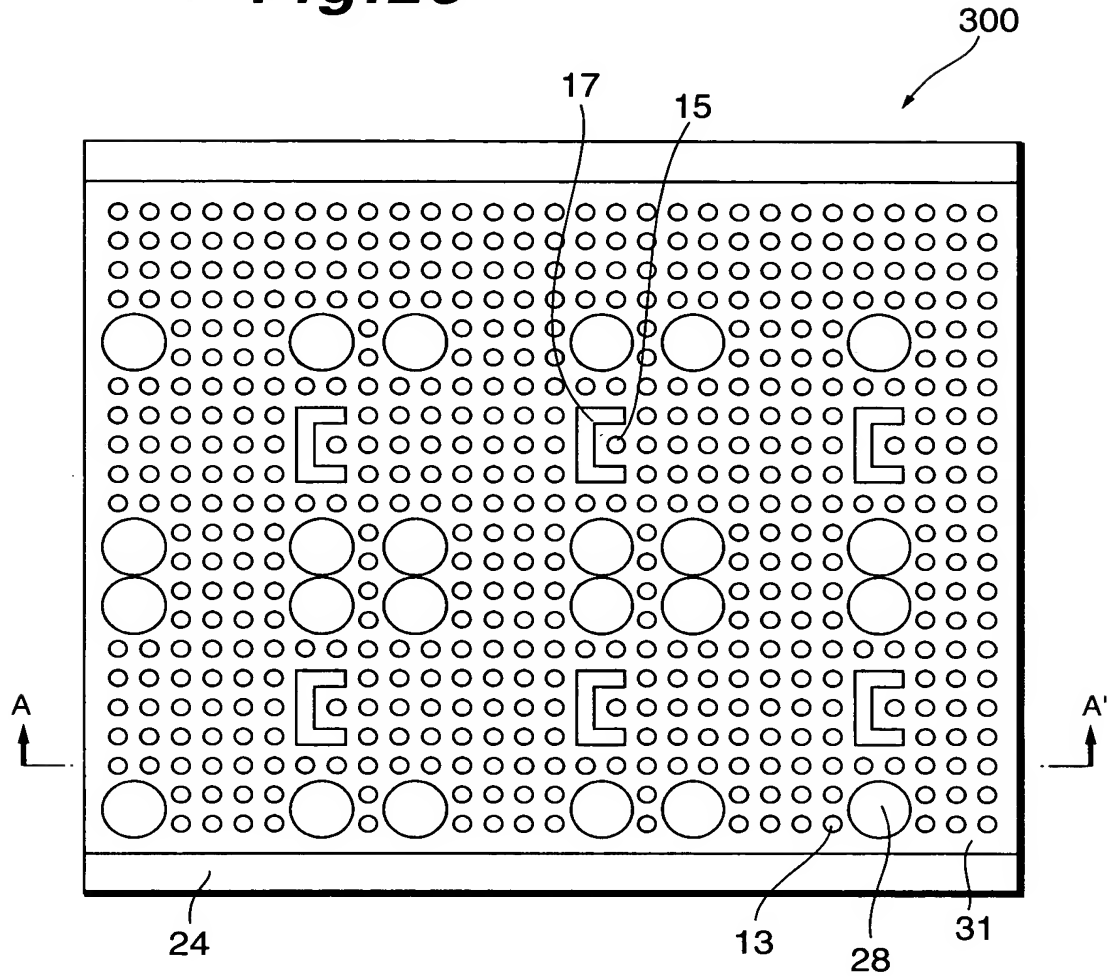


Fig.24

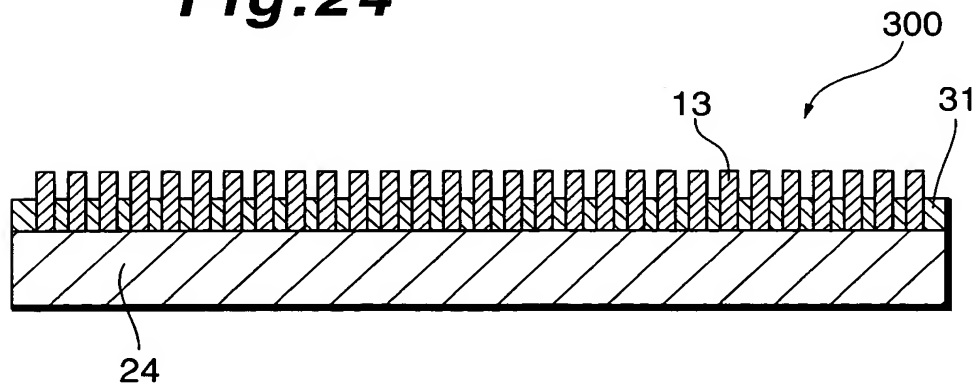


Fig. 25

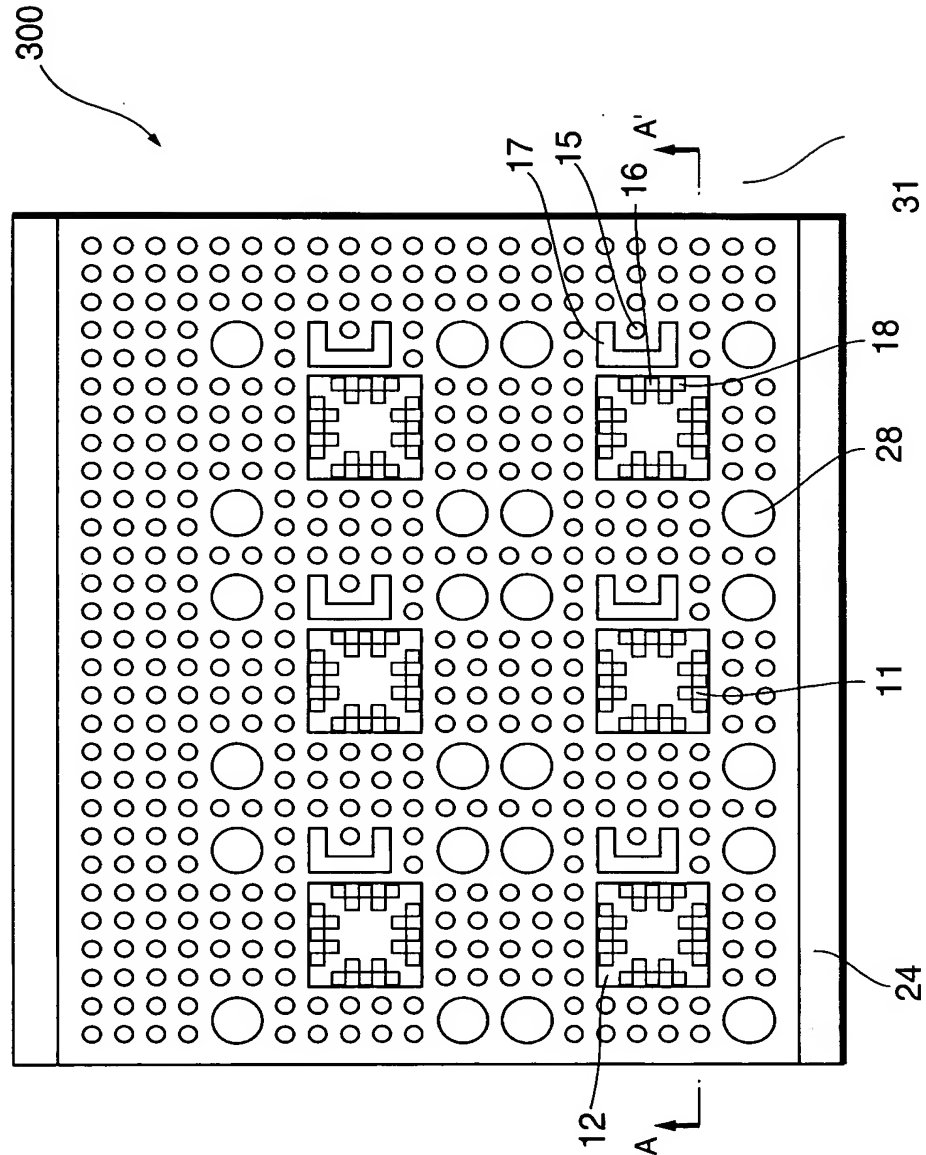


Fig.26

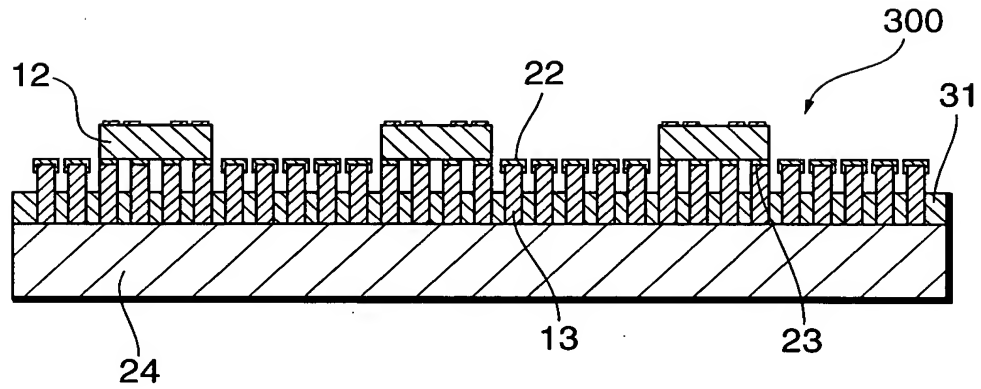


Fig.27

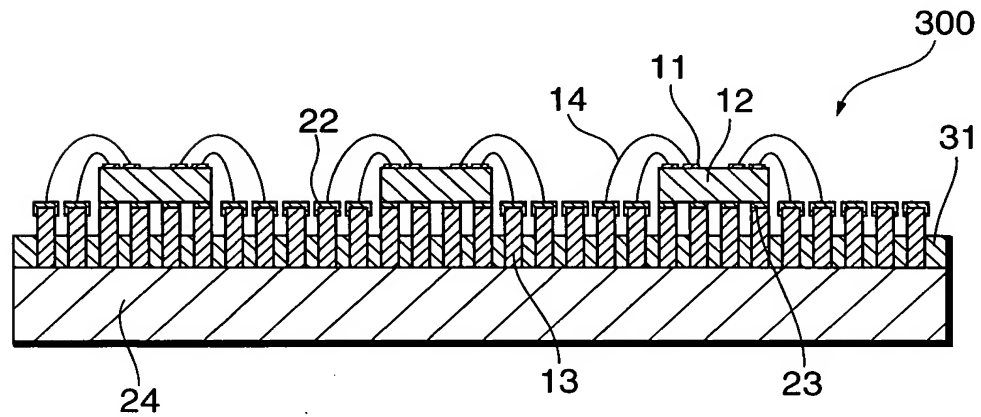
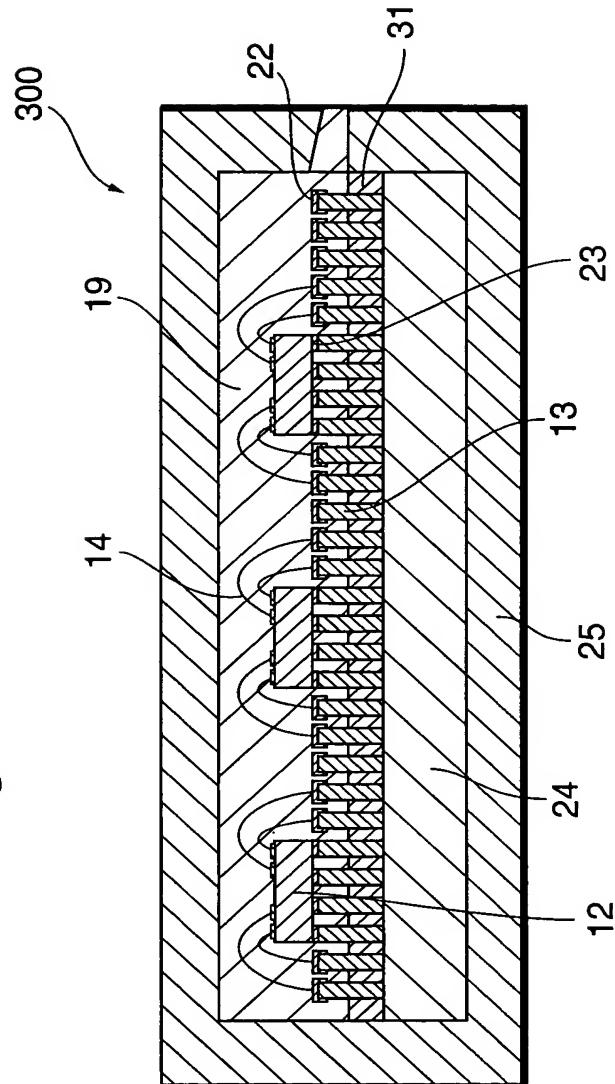


Fig. 28



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Fig.29

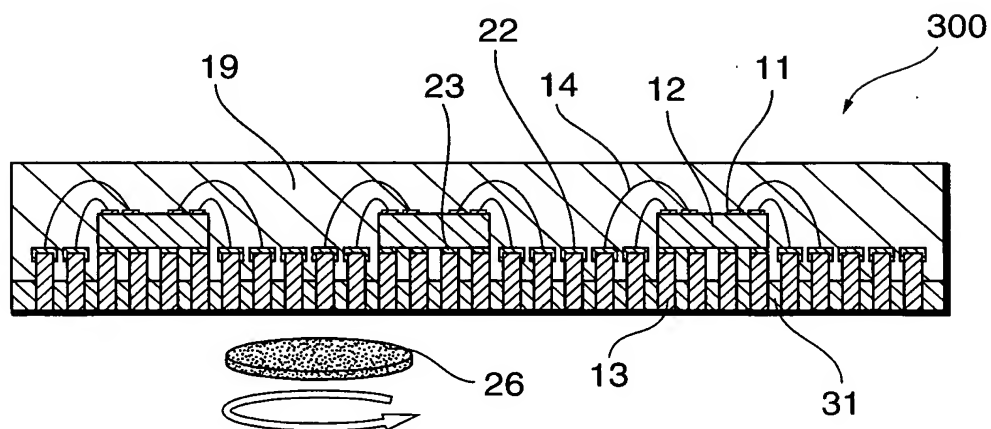


Fig.30

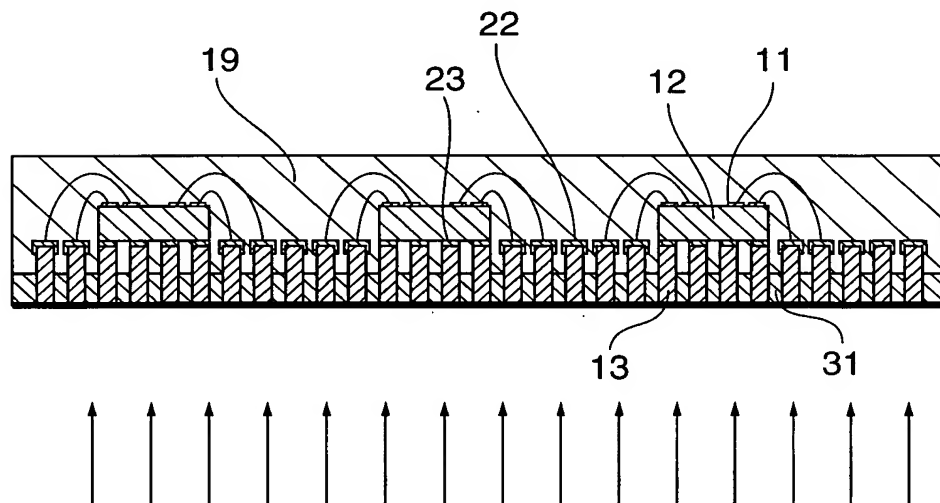


Fig.31

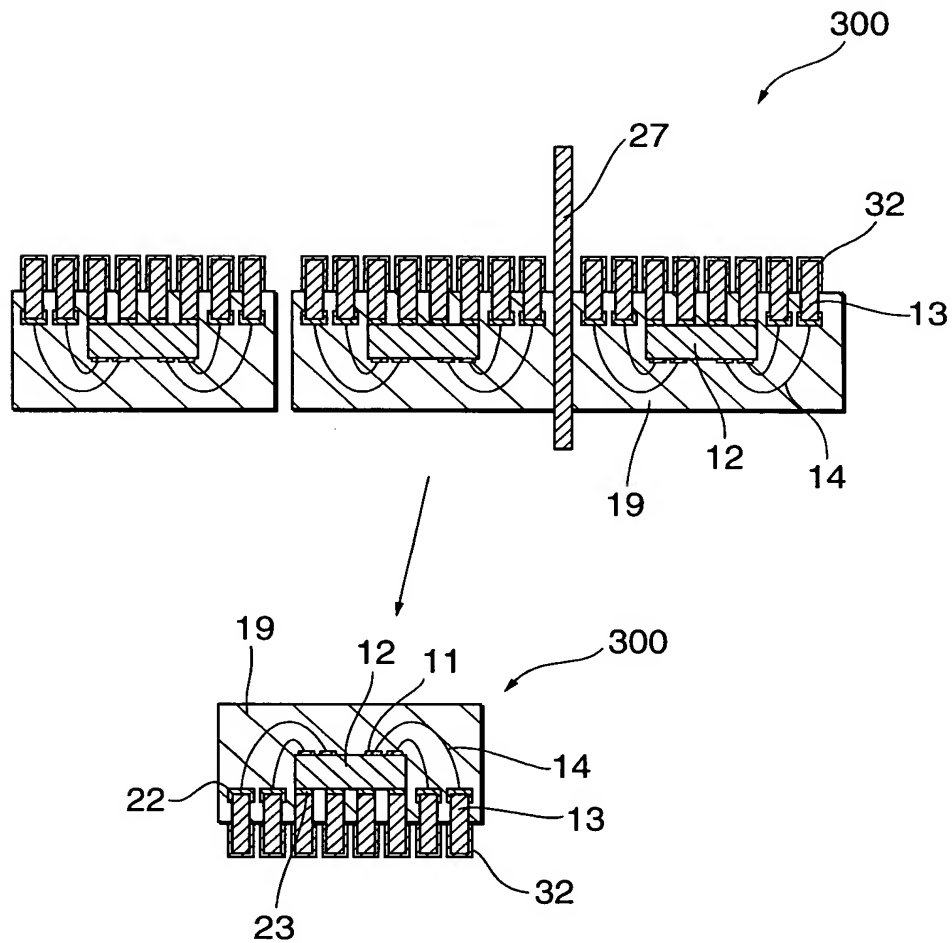


Fig.32

